Amendments to the Claims

Claims 1-31 (cancelled).

32. (currently amended) A semiconductor device for suppressing an external transient voltage, comprising an insulated gate bipolar transistor (IGBT) having a gate terminal and a first conduction terminal coupled to receive the external transient voltage, first and second diodes coupled in a back to back fashion between the gate and first conduction terminals, and a second conduction terminal to shunt a surge current flowing through the first conduction terminal in response to the external transient voltage exceeding a predetermined level.

33. (previously presented) The semiconductor device of claim 32, further comprising a semiconductor substrate having a top surface for forming the first conduction terminal and the gate terminal of the IGBT.

34. (currently amended) The semiconductor device of claim 33, wherein the semiconductor substrate includes:

a body region of a first conductivity type for inverting to form a channel of the IGBT;

an emitter region formed at the top ~~first~~ surface for receiving the surge current from the first conduction terminal; and

a drift region having a second conductivity type and coupled to the channel for conducting the surge current.

35. (previously presented) The semiconductor device of claim 34, wherein the semiconductor substrate further includes a collector region of the first conductivity type formed adjacent to the drift region for routing the surge current between the drift region and the second conduction terminal.

36. (previously presented) The semiconductor device of claim 35, wherein the collector region is formed on the top surface of the semiconductor substrate.

37. (previously presented) The semiconductor device of claim 35, wherein the semiconductor substrate has a bottom surface for forming the collector region and the second conduction terminal.

38. (previously presented) The semiconductor device of claim 37, further comprising a semiconductor package having a die flag for mounting the semiconductor substrate, wherein the collector region is electrically coupled to the die flag for routing the surge current to an external node.

39. (previously presented) The semiconductor device of claim 38, wherein the semiconductor package further includes a bonding wire coupled between the gate terminal and the die flag.

40. (previously presented) The semiconductor device of claim 37, further comprising a collection region of the first conductivity type that is coupled to the first conduction terminal and formed at the top surface for

collecting minority carriers injected from the collector region.

Claim 41 (cancelled).

42. (currently amended) The semiconductor device of claim [[41,]] 34, wherein the first and second diodes are formed in a semiconductor layer disposed on the top surface of the semiconductor substrate.

43. (previously presented) The semiconductor device of claim 42, wherein a region of the semiconductor layer overlies the channel to form the gate terminal of the IGBT.

44. (previously presented) The semiconductor device of claim 42, wherein the semiconductor layer is formed with polycrystalline silicon.

45. (previously presented) The semiconductor device of claim 44, wherein the external transient voltage turns on the IGBT to conduct the surge current between the first and second conduction terminals at a level greater than about five amperes.

46. (previously presented) The semiconductor device of claim 45, wherein the IGBT limits a magnitude of the external voltage transient to a value less than about five volts.

47. (new) A semiconductor device for suppressing an external transient voltage, comprising an insulated gate bipolar transistor (IGBT) having a gate terminal and a first conduction terminal coupled to receive the external transient voltage and a second conduction terminal to shunt a surge current flowing through the first conduction terminal in response to the external transient voltage exceeding a predetermined level, wherein the semiconductor device further includes:

a semiconductor substrate having a top surface for forming the first conduction terminal and the gate terminal of the IGBT and a bottom surface;

a body region of a first conductivity type formed in the semiconductor substrate for inverting to form a channel of the IGBT;

an emitter region formed at the top surface for receiving the surge current from the first conduction terminal;

a drift region having a second conductivity type and coupled to the channel for conducting the surge current;

a collector region of the first conductivity type formed adjacent to the drift region for routing the surge current between the drift region and the second conduction terminal; and

a semiconductor package having a die flag for mounting the semiconductor substrate, wherein the collector region is electrically coupled to the die flag for routing the surge current to an external node.

48. (new) The semiconductor device of claim 47 further comprising first and second diodes coupled in a back to back fashion between the gate and first conduction terminals.